



# Datasheet

## Citiroc1A



Citiroc is a 32-channel front-end ASIC designed to readout silicon photo-multipliers (SiPM).

Citiroc allows triggering down to 1/3 pe and provides the charge measurement with a good noise rejection. Moreover, Citiroc outputs the 32-channel triggers with a high accuracy (100 ps).

An adjustment of the SiPM high-voltage is possible using a channel-by-channel DAC connected to the ASIC inputs. That allows a fine SiPM gain and dark noise adjustment at the system level to correct for the non-uniformity of SiPMs.

Timing measurement down to 100 ps RMS jitter is possible along with 1% linearity energy measurement up to 2500 p.e. The power consumption is about 2mW/channel, excluding ASIC outing buffer.

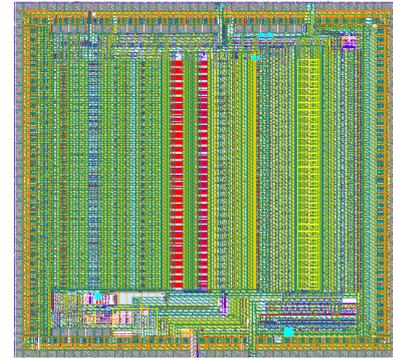


Figure 1 - ASIC layout

Parameter	Value
Detector Read-Out	SiPM, SiPM array
Number of Channels	32
Signal Polarity	Positive
Sensitivity	Trigger on 1/3 of photo-electron
Timing Resolution	100 ps RMS on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ $10^6$ SiPM gain
Packaging & Dimension	Naked die – 4.1 x 4.1mm – 16.5mm <sup>2</sup> / TQFP 160
Power Consumption	60mW Analogue Core (excluding outing buffer) 95mW Asic Outing (all outputs on)
Inputs	32 voltage inputs with independent SiPM HV adjustments
Outputs	32 trigger outputs 1 multiplexed charge output 1 ASIC trigger output (Trigger OR)
Internal Programmable Features	32 HV adjustment for SiPM (16x8bits), Trigger Threshold Adjustment (10bits), channel by channel gain tuning, 32 Trigger Masks, Channel by Channel Output Enable, Trigger Latch

Table 1 – ASIC main parameters



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### Learn more about Citiroc

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# Datasheet Citiroc1A



## Table of content

1	General description.....	3
2	ASIC pinout.....	5
2.1	Pin type description .....	5
2.2	LQFP 160 packaging.....	6
2.2.1	Package layout & mechanics.....	6
2.2.2	Pin type description .....	7
2.3	TFBGA 353 package.....	10
2.3.1	Package layout & mechanics.....	10
3	ASIC programmable parameters .....	15
3.1	General description.....	15
3.2	Slow control register parameters.....	15
3.3	Probe register parameters.....	17
4	ASIC Front-end .....	17
4.1	Input DACs.....	17
4.2	Preamplifiers.....	18
4.3	Slow Shaper.....	18
4.4	Trigger line.....	19
4.5	Track and hold.....	21
4.6	Peak detector.....	22
5	ASIC Back-end.....	23
5.1	Direct digital Outputs.....	23
5.2	Analogue chip read out.....	23
5.3	Output (Multiplexed Latches): Hit Register ..	23
5.4	Power pulsing and ON/OFF functions.....	24

## Table of figures

Figure 1 - ASIC layout.....	1
Figure 2 - General ASIC block scheme.....	3
Figure 3 - North west Citiroc 1A ball-out.....	10
Figure 4 - North east Citiroc 1A ball-out.....	11
Figure 5 - South west Citiroc 1A ball-out.....	12
Figure 6 - South east Citiroc1A ball-out.....	13
Figure 7 - Citiroc1A TFBGA353 mechanics .....	14
Figure 8: Slow control chronogram and explanation...	15
Figure 9 – 2 different schemes of the SiPM connection to the ASIC.....	18
Figure 10 – High gain and low gain voltage sensitive preamplifier.....	18
Figure 11 – Slow shaper schematic.....	19
Figure 12 – Fast Shaper schematic.....	20
Figure 13 – Val Evt signal effect .....	20
Figure 14 - – Trigger output using Latch.....	20
Figure 15 – Trigger output in direct discriminator mode .....	21
Figure 16 – Schematic of track and hold cell.....	21
Figure 17– Standard Track & Hold working mode.....	21
Figure 18 – Peak detector working mode.....	22
Figure 19– Read Register.....	23
Figure 20 - Read Register.....	24
Table 1 – ASIC main parameters .....	1
Table 2 – pin type description .....	5
Table 3 – LQFP 160 pinout.....	9
Table 5 – slow control register parameters.....	17
Table 6 – Probe register parameters.....	17
Table 7– Slow shaper peaking time value vs slow control parameters.....	19
Table 8 – Power mode truth table.....	24



# Datasheet Citiroc1A



## 1 General description

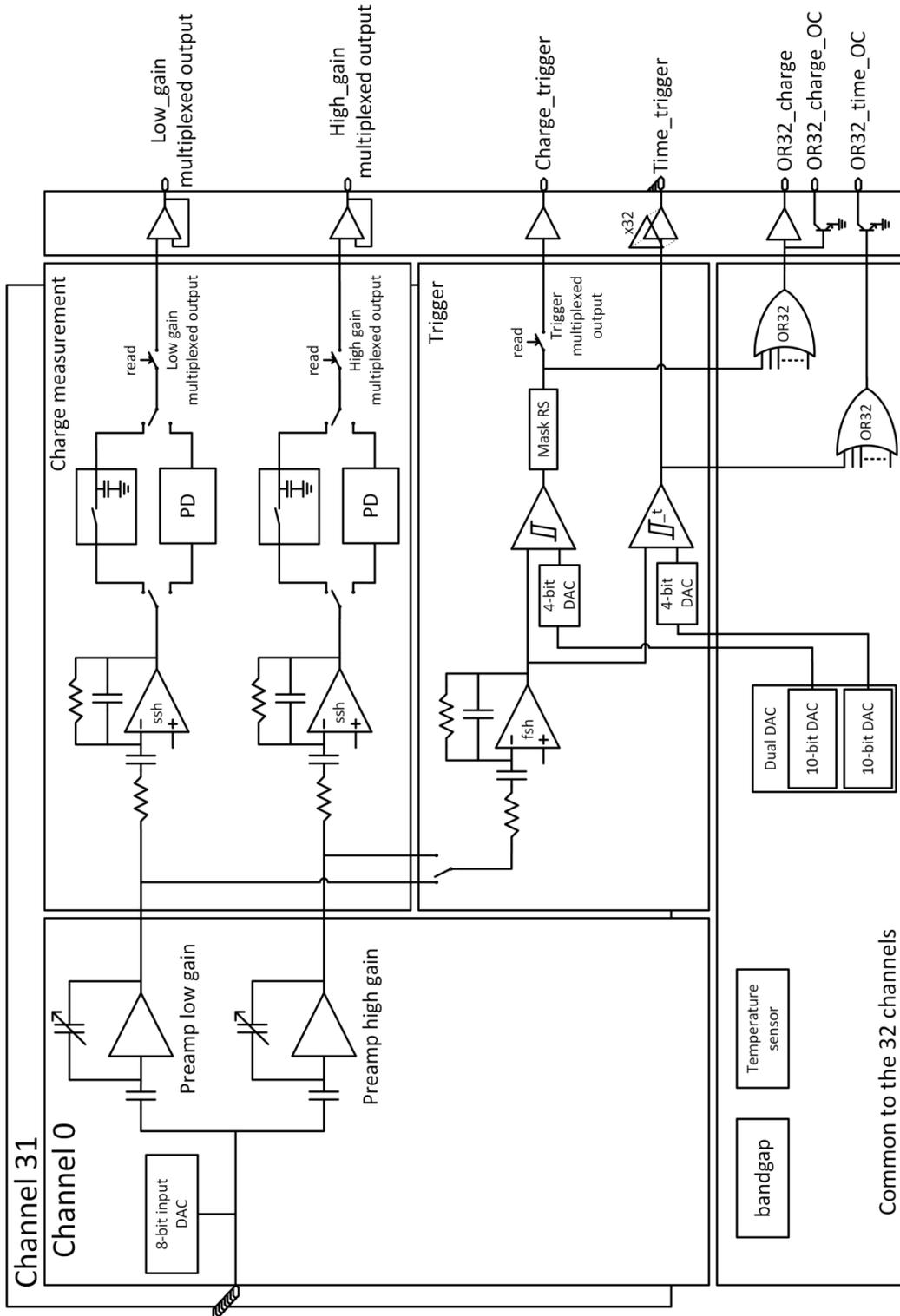


Figure 2 - General ASIC block scheme



# Datasheet

## Citiroc1A



CITIROC is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors. Each of the 32 inputs features a low power 4.5V range 8-bit DAC to easily adjust the SiPM high voltage channel by channel and improve the gain and noise uniformity of the system.

The analogue core is sensitive to positive SiPM signals. For each channel, two parallel AC coupled voltage preamplifiers ensure the read out of the charge from 160 fC to 320 pC (ie. 1 to 2000 photoelectrons with SiPM Gain =  $10^6$ , with a photoelectron to noise ratio of 10). Two variable shapers are used to reduce noise; each of them has an adjustable time constant from 12.5 ns to 87.5 ns to allow the user to minimize the noise depending on the final application. A trigger line is available from the high gain preamplifier or low gain preamplifier. It is composed of a 15 ns peaking time fast shaper followed by two discriminators. The first one provides the trigger (OR32) and is also used for the "hit register", and the second one provides accurate event time information of each channel. Indeed, the 32 discriminators outputs are available. Thresholds are set coarsely by two internal common for the 32 channels 10-bit DAC and then set finely channel by channel by individual 4-bit DAC.

A bias feature provides the current to the 32 channels. Each stage of all channels can be disabled independently to save power whenever not used. A "power pulsing" capability ensures a maximum power saving when the chip is not aimed to detect during dead time of the system. CITIROC has been designed to ensure maximum versatility and easiness to use for fast prototyping. It can be easily programmed using a reliable shift register. A probe system is implemented to allow debug and characterization by outputting any analogue point inside the chip using a unique multiplexed output.



# Datasheet Citiroc1A



## 2 ASIC pinout

Citiroc is available in a LQFP 160 or TFBGA 353 package.

### 2.1 Pin type description

Pin type	Description	Connection
Power	Power or Ground pin	Decoupling advised
Analogue input	Analogue signal input	See specifics
Analogue output	Analogue signal output	External buffering required if cable driving
Analogue bias	Analogue bias connection. Bias is internal and can be tuned externally through these pins	Not mandatory if not specifically specified
Digital input	Digital input connection	TTL levels
Digital output	Digital output connection	TTL levels
Digital output OC	Open Collector digital output connection	External pull-up resistor required
Digital input LVDS	LVDS pair connection	See LVDS norm, matching resistor outside ASIC
Digital output LVDS	LVDS pair connection	See LVDS norm, matching resistor outside ASIC

Table 2 – pin type description

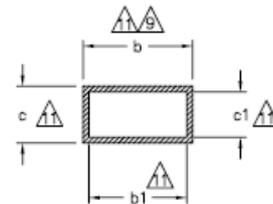
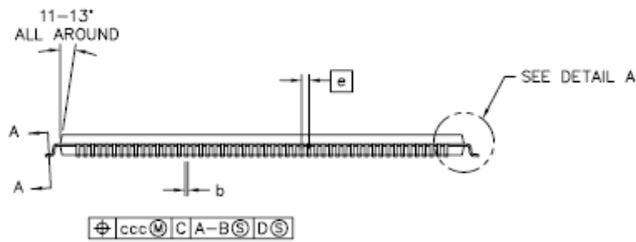
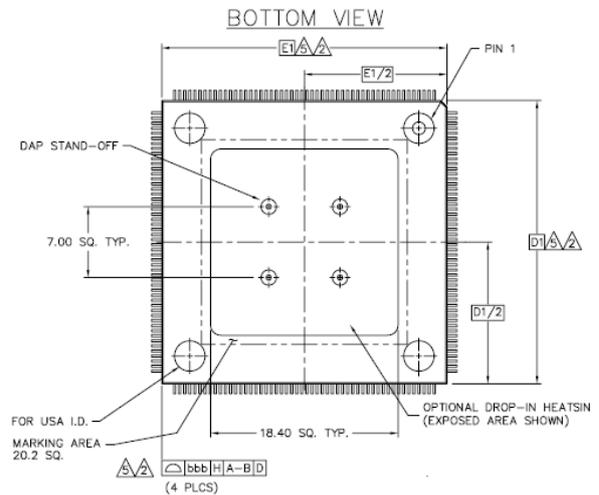
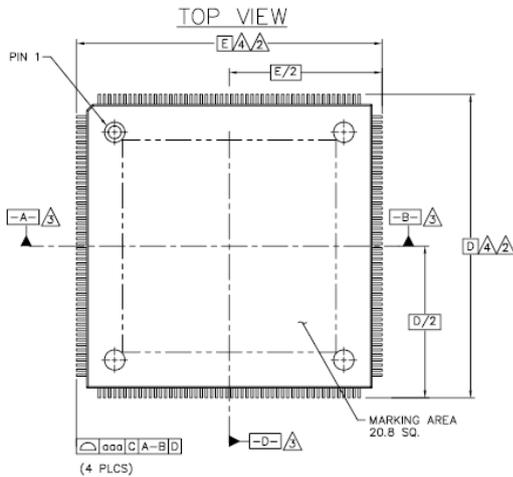


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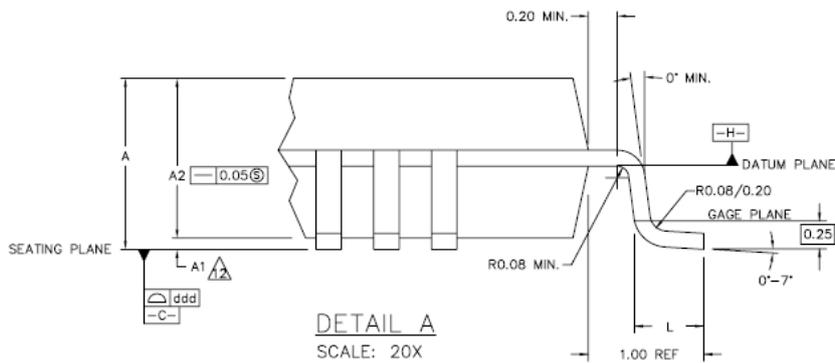


## 2.2 LQFP 160 packaging

### 2.2.1 Package layout & mechanics



SECTION A-A  
SCALE: 40:1



DETAIL A  
SCALE: 20X

SYMBOL	LEAD COUNT; FOOT PRINT			NOTE
	MIN.	NOM.	MAX.	
A	----	----	1.60	
A1	0.05	----	0.15	
A2	1.35	1.40	1.45	
D	30.00 BSC			
D1	28.00 BSC			
E	30.00 BSC			
E1	28.00 BSC			
L	0.45	0.60	0.75	
e	0.65 BSC			
b	0.22	----	0.38	
b1	0.22	0.28	0.33	
c	0.09	----	0.20	
c1	0.09	----	0.16	
Tolerances of form and position				
aaa	0.20			
bbb	0.20			
ccc	0.12			
ddd	0.08			



# Datasheet

## Citiroc1A



### 2.2.2 Pin type description

Pin #	Pin name	Pin type	Description	Connection
1	vssi	Power	Analogue part Bulk	to GND
2	vref_iGen_dac_5V	Analogue Bias	8-bit DAC reference bias voltage (for 4,5V dynamic range)	100nF
3	ib_dac_4b	Analogue Bias		
4	in<0>	Analogue Input	Channel 0 input	
5	in<1>	Analogue Input	Channel 1 input	
6	in<2>	Analogue Input	Channel 2 input	
7	in<3>	Analogue Input	Channel 3 input	
8	in<4>	Analogue Input	Channel 4 input	
9	in<5>	Analogue Input	Channel 5 input	
10	in<6>	Analogue Input	Channel 6 input	
11	in<7>	Analogue Input	Channel 7 input	
12	vdda_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
13	in<8>	Analogue Input	Channel 8 input	
14	in<9>	Analogue Input	Channel 9 input	
15	in<10>	Analogue Input	Channel 10 input	
16	in<11>	Analogue Input	Channel 11 input	
17	in<12>	Analogue Input	Channel 12 input	
18	in<13>	Analogue Input	Channel 13 input	
19	in<14>	Analogue Input	Channel 14 input	
20	in<15>	Analogue Input	Channel 15 input	
21	vssi	Power	Analogue part Bulk	to GND
22	in<16>	Analogue Input	Channel 16 input	
23	in<17>	Analogue Input	Channel 17 input	
24	in<18>	Analogue Input	Channel 18 input	
25	in<19>	Analogue Input	Channel 19 input	
26	in<20>	Analogue Input	Channel 20 input	
27	in<21>	Analogue Input	Channel 21 input	
28	in<22>	Analogue Input	Channel 22 input	
29	in<23>	Analogue Input	Channel 23 input	
30	vdda_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
31	in<24>	Analogue Input	Channel 24 input	
32	in<25>	Analogue Input	Channel 25 input	
33	in<26>	Analogue Input	Channel 26 input	
34	in<27>	Analogue Input	Channel 27 input	
35	in<28>	Analogue Input	Channel 28 input	
36	in<29>	Analogue Input	Channel 29 input	
37	in<30>	Analogue Input	Channel 30 input	
38	in<31>	Analogue Input	Channel 31 input	
39	ib_temp	Analogue Bias		
40	out_temp	Analogue Output		
41	vssi	Power	Analogue part Bulk	to GND
42	NC_bottom			
43	vdda_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
44	vssa	Power	Analogue part Bulk	to GND
45	v_bg	Analogue Output	BandGap output	
46	vdd_dac	Power	Analogue (10-bit DAC) Power Supply	to 3.3V
47	gnd_dac	Power	Analogue (10-bit DAC) Ground	to GND
48	vth	Analogue Output	10-bit DAC output (Trigger Discriminator Threshold)	
49	iref_dac	Analogue Bias	10-bit DAC bias current	
50	vref_ssh_lg	Analogue Bias	Low Gain Slow Shapers bias voltage	
51	vth_t	Analogue Output	10-bit DAC output (2nd Trigger Discriminator Threshold)	
52	vref_ssh_hg	Analogue Bias	High Gain Slow Shapers bias voltage	
53	vref_fs	Analogue Bias	Fast Shapers bias voltage	
54	vdd_fs	Power	Analogue (Fast Shaper) Power Supply	to 3.3V
55	vdd_sca	Power	Analogue (Switched Capacitor Array) Power Supply	to 3.3V



# Datasheet Citiroc1A



56	gnd_fs	Power	Analogue (Fast Shaper) Ground	to GND
57	gnd_capa_sca_hg	Power	Analogue SCA capacitors Ground (High Gain)	to GND
58	gnd_capa_sca_lg	Power	Analogue SCA capacitors Ground (Low Gain)	to GND
59	gnd_sca	Power	Analogue (Switched Capacitor Array) Ground	to GND
60	vssa	Power	Analogue part Bulk	to GND
	vssm	Power	Mixed part Bulk	to GND
61	out_hg	Analogue Output	High Gain Slow Shaper Multiplexed Output (Hi Z when not Ch. selected)	
62	out_lg	Analogue Output	Low Gain Slow Shaper Multiplexed Output (Hi Z when not Ch. selected)	
63	out_probe	Analogue Output	Analogue Probe Output	
64	ib_otaq	Analogue Bias	Analogue outputs OTA bias	
65	vssm	Power	Mixed part Bulk	to GND
66	vssd	Power	Digital part Bulk	to GND
67	gndd	Power	Digital (LVDS receivers & digital parts) Ground	to GND
68	vddd	Power	Digital (LVDS receivers & digital parts) Power Supply	to 3.3V
69	ib_rec	Analogue Bias	LVDS receiver bias current	
70	resetb_pa	Digital Input	Charge PreAmp Reset Signal	Active L
71	rstb_PSC	Digital Input	Peak Detector Cell reset	Active L
72	pwr_on	Digital Input	Power Pulsing Control	Active H
73	Raz_Ch_n_p	Digital (LVDS) Input	Erase RS cell	Active H
74	Raz_Ch_n_n			
75	Val_Evt_p	Digital (LVDS) Input	Acquisition window (valid events)	Active H
76	Val_Evt_n			
77	digital_output/hit_mux	Digital Output	Digital (Triggers) Multiplexed Output (Hi Z when not Ch. selected)	
78	OR32	Digital Output	OR of the 32 triggers	
79	select	Digital Input	Select Slow Control Register (1) or Probe Register (0)	
80	NOR32_oc	OC Digital Output	NOR of the 32 triggers (Open Collector Output)	
81	vssd	Power	Digital part Bulk	to GND
82	PS_global_trig	Digital Input		
83	NOR32T_oc	OC Digital Output	NOR of the 2nd threshold 32 triggers (Open Collector Output)	
84	T<31>	Digital Output	Channel 31 Trigger Output	
85	T<30>	Digital Output	Channel 30 Trigger Output	
86	T<29>	Digital Output	Channel 29 Trigger Output	
87	T<28>	Digital Output	Channel 28 Trigger Output	
88	T<27>	Digital Output	Channel 27 Trigger Output	
89	T<26>	Digital Output	Channel 26 Trigger Output	
90	T<25>	Digital Output	Channel 25 Trigger Output	
91	T<24>	Digital Output	Channel 24 Trigger Output	
92	T<23>	Digital Output	Channel 23 Trigger Output	
93	T<22>	Digital Output	Channel 22 Trigger Output	
94	T<21>	Digital Output	Channel 21 Trigger Output	
95	T<20>	Digital Output	Channel 20 Trigger Output	
96	T<19>	Digital Output	Channel 19 Trigger Output	
97	T<18>	Digital Output	Channel 18 Trigger Output	
98	T<17>	Digital Output	Channel 17 Trigger Output	
99	T<16>	Digital Output	Channel 16 Trigger Output	
100	vlo	Power	Digital Output Buffer Minimum Power Supply	Positive
101	vssd	Power	Digital part Bulk	to GND
102	vhi	Power	Digital Output Buffer Maximum Power Supply	
103	T<15>	Digital Output	Channel 15 Trigger Output	
104	T<14>	Digital Output	Channel 14 Trigger Output	
105	T<13>	Digital Output	Channel 13 Trigger Output	
106	T<12>	Digital Output	Channel 12 Trigger Output	
107	T<11>	Digital Output	Channel 11 Trigger Output	
108	T<10>	Digital Output	Channel 10 Trigger Output	
109	T<9>	Digital Output	Channel 9 Trigger Output	
110	T<8>	Digital Output	Channel 8 Trigger Output	
111	T<7>	Digital Output	Channel 7 Trigger Output	
112	T<6>	Digital Output	Channel 6 Trigger Output	



# Datasheet

## Citiroc1A



113	T<5>	Digital Output	Channel 5 Trigger Output	
114	T<4>	Digital Output	Channel 4 Trigger Output	
115	T<3>	Digital Output	Channel 3 Trigger Output	
116	T<2>	Digital Output	Channel 2 Trigger Output	
117	T<1>	Digital Output	Channel 1 Trigger Output	
118	T<0>	Digital Output	Channel 0 Trigger Output	
119	digital_probe	Digital Output		
120	PS_modeb_ext	Digital Input		
121	vssd	Power	Digital part Bulk	to GND
122	gndd	Power		to GND
123	vddd	Power	Digital (LVDS receivers & digital parts) Power Supply	to 3.3V
124	load_sc	Digital Input	Slow Control Register Load Signal	Active ↑
125	srou_sr	Digital Output	Selected Register Output	
126	srin_sr	Digital Input	Selected Register Input	
127	clk_sr	Digital Input	Selected Register Clock	Active ↑
128	rstb_sr	Digital Input	Selected Register Reset	Active L
129	vssd	Power	Digital part Bulk	to GND
130	vssm	Power	Mixed part Bulk	to GND
131	hold_lg	Digital Input	Analogue Memory Hold Signal for High Gain	
132	resetb_read	Digital Input	Read Register Reset	Active H
133	srou_read	Digital Output	Read Register Output	
134	srin_read	Digital Input	Read Register Input	
135	clk_read	Digital Input	Read Register Clock	
136	hold_hg	Digital Input	Analogue Memory Hold Signal for Low Gain	Active H
137	vdd_discri	Power	Analogue (Discriminator) Power Supply	to 3.3V
138	gnd_discri	Power	Analogue (Discriminator) Ground	to GND
	vssm	Power	Mixed part Bulk	to GND
139	vssa	Power	Analogue part Bulk	to GND
140	gnd_ssh	Power	Analogue (Slow Shaper) Ground	to GND
141	vdd_ssh	Power	Analogue (Slow Shaper) Power Supply	to 3.3V
142	vdd_sc	Power	Digital (Slow Control Register) Power Supply	to 3.3V
143	gnd_sc	Power	Digital (Slow Control Register) Ground	to GND
144	ib_sca	Analogue Bias	SCA bias current	
145	gnd_capa	Power	Analogue (Slow Shaper Capacitor) Ground	to GND
146	ib_1nA_peak	Analogue Bias		
147	ibo_peak	Analogue Bias		
148	ibi_peak	Analogue Bias		
149	in_calib	Analogue Input	Calibration input	
150	gnd_pa	Power	Analogue (PreAmplifier) Ground	to GND
151	vssa	Power		
152	vdd_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
153	vdda_pa	Power	Analogue (PreAmplifier) Power Supply	to 3.3V
154	vssi	Power	Analogue part Bulk	to GND
155	NC_top			
156	gnd_dac_5V	Power	Analogue (8-bit Digital to Analogue Convertor) Ground	to GND
157	vref_dac_5V	Analogue Bias	8-bit DAC reference bias voltage	
158	vdd_dac_5V	Power	Analogue (8-bit Digital to Analogue Convertor) Power Supply	to 5V
159	ib_dac_5V	Analogue Bias	8-bit DAC bias voltage	
160	ibi_discri_t	Analogue Bias		

Table 3 – LQFP 160 pinout



# Datasheet Citiroc1A



## 2.3 TFBGA 353 package

### 2.3.1 Package layout & mechanics

	1	2	3	4	5	6	7	8	9	10	11	12
<b>A</b>	ib_1nA_dac	ibo_ota_dac	ibi_ota_dac	ibi_pa_hg	ibo_pa_hg	ibmin_pa	ibo_pa_lg	ib_suiv_r_c_hg	ib_suiv_r_c_lg	ibi_ssh_lg	NC	ibo_ssh_hg
<b>B</b>	in0	ibo_discr_i_t	ib_dac_5V	vref_dac_5V	NC_top	ibm_pa_hg	ibm_pa_lg	ibi_pa_lg	ib_1nA_peak	ib_sca	ibi_ssh_hg	ibfol_discr_i_t
<b>C</b>	in1	vref_iGen_dac_5V										
<b>D</b>	in2	ib_dac_4b										
<b>E</b>	in4	in3			VDDI	VDDI	VDDI	VDDI	in_calib	ibi_peak	ibo_peak	ibi_fs
<b>F</b>	in6	in5			VDDI	VDDI	VDDI	VDDI	VDDA	VDDA	VDDA	VDDA
<b>G</b>	in8	in7			VDDI	VDDI						
<b>H</b>	in10	in9			VDDI	VDDI		VSS	VSS	VSS	VSS	VSS
<b>J</b>	in12	in11			VDDI	VDDI		VSS	VSS	VSS	VSS	VSS
<b>K</b>	in13	VDDI			VDDI	VDDI		VSS	VSS	VSS	VSS	VSS
<b>L</b>	in14	VDDI			VDDI	VDD_5V		VSS	VSS	VSS	VSS	VSS
<b>M</b>	in16	in15			VDDI	VDD_5V		VSS	VSS	VSS	VSS	VSS

Figure 3 - North west Citiroc 1A ball out



# Datasheet Citiroc1A

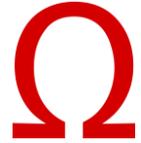


12	13	14	15	16	17	18	19	20	21	22	23	
ibo_ssh_hg	ibo_fs	clk_read	srout_read	ibo_discr_i	NC	clk_sr	srin_sr	PS_mod eb_ext	digital_p robe	T1	T3	<b>A</b>
ibfol_dis cri_t	ib_suiv_f s	ibm_disc ri_t	ibm_disc ri	NC	ibi_discr _t	rstb_sr	srout_sr	load_sc	T0	T2	T4	<b>B</b>
										NC	T5	<b>C</b>
										NC	T6	<b>D</b>
ibi_fs	hold_hg	srin_read	resetb_re ad	ibi_discr_i	VDDD	VDDD	VDDD			NC	T7	<b>E</b>
VDDA	VDDA	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD			NC	T8	<b>F</b>
						VDDD	NC			NC	T9	<b>G</b>
VSS	VSS	VSS	VSS	VSS		VDDD	NC			NC	T10	<b>H</b>
VSS	VSS	VSS	VSS	VSS		VDDD	NC			NC	T11	<b>J</b>
VSS	VSS	VSS	VSS	VSS		VDDD	NC			NC	T12	<b>K</b>
VSS	VSS	VSS	VSS	VSS		vhi	vhi			T13	T14	<b>L</b>
VSS	VSS	VSS	VSS	VSS		VDDD	VDDD			T15	T16	<b>M</b>

Figure 4 - Nortn east Citiroc 1A ball-out



# Datasheet Citiroc1A



<b>M</b>	in16	in15			VDDI	VDD_5V		VSS	VSS	VSS	VSS	VSS
<b>N</b>	in17	VDDI			VDDI	VDD_5V		VSS	VSS	VSS	VSS	VSS
<b>P</b>	in18	VDDI			VDDI	VDDI		VSS	VSS	VSS	VSS	VSS
<b>R</b>	in19	in20			VDDI	VDDI		VSS	VSS	VSS	VSS	VSS
<b>T</b>	in21	in22			VDDI	VDDI		VSS	VSS	VSS	VSS	VSS
<b>U</b>	in23	in24			VDDI	VDDI						
<b>V</b>	in25	in26			VDDI	VDDI	VDDA	VDDA	VDDA	VDDA	VDDA	VDDA
<b>W</b>	in27	in28			VDDI	VDDI	VDDA	VDDA	NC	NC	VDDA	NC
<b>Y</b>	in29	ib_temp										
<b>AA</b>	in30	out_tem p										
<b>AB</b>	in31	out_pro be_dac_ 5V	vg_pa_h g	vref_dac	ibi_dac	iref_dac	vref_ssh _lg	vref_ssh _hg	NC	NC	NC	NC
<b>AC</b>	ib_ota_b g	vg_pa_lg	v_bg	va_pa	vth	ibo_dac	vth_t	vref_fs	NC	NC	out_hg	out_lg
	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>	<b>5</b>	<b>6</b>	<b>7</b>	<b>8</b>	<b>9</b>	<b>10</b>	<b>11</b>	<b>12</b>

Figure 5 - South west Citiroc 1A ball-out



# Datasheet Citiroc1A

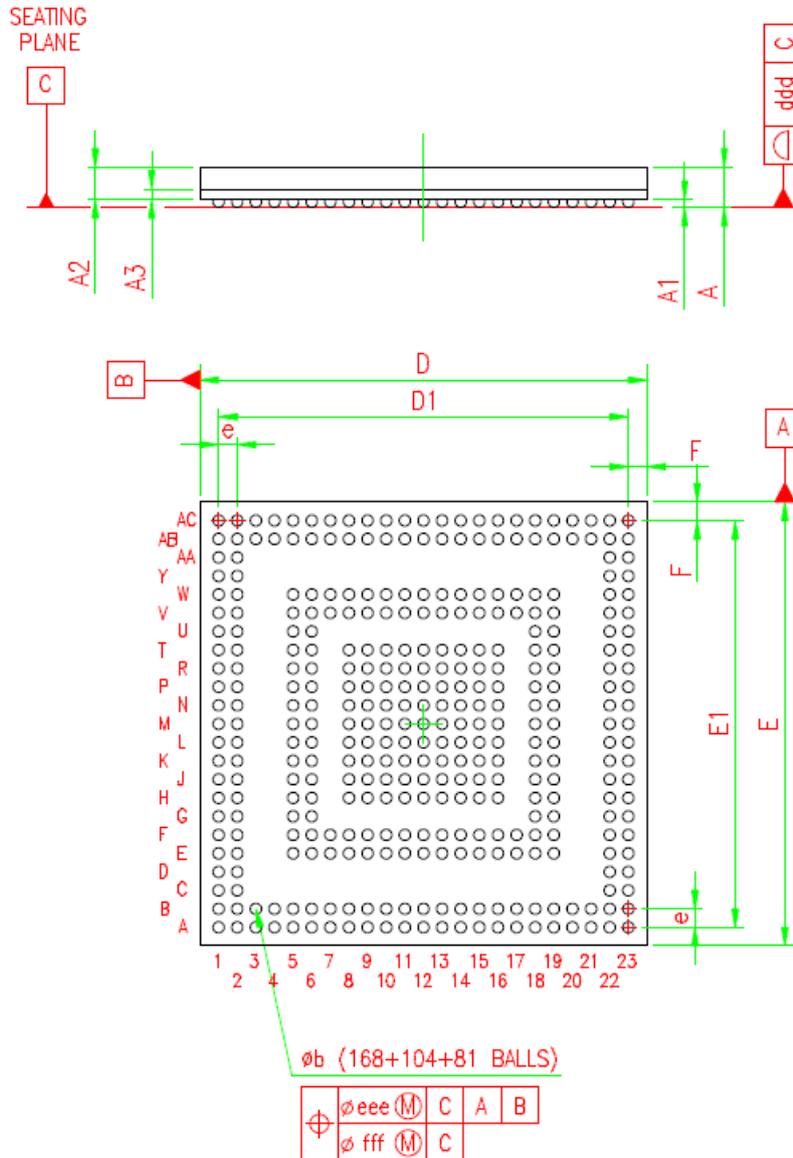


VSS	VSS	VSS	VSS	VSS		VDDD	VDDD			T15	T16	<b>M</b>
VSS	VSS	VSS	VSS	VSS		vlo	vlo			T17	T18	<b>N</b>
VSS	VSS	VSS	VSS	VSS		VDDD	NC			NC	T19	<b>P</b>
VSS	VSS	VSS	VSS	VSS		VDDD	NC			NC	T20	<b>R</b>
VSS	VSS	VSS	VSS	VSS		VDDD	NC			NC	T21	<b>T</b>
						VDDD	NC			NC	T22	<b>U</b>
VDDA	VDDA	VDDA	VDDA	VDDD	VDDD	VDDD	VDDD			NC	T23	<b>V</b>
NC	NC	NC	NC	NC	NC	VDDD	VDDD			NC	T24	<b>W</b>
										NC	T25	<b>Y</b>
										NC	T26	<b>AA</b>
NC	ib_otaq	NC	ib_rec	rstb_PSC	OR32	digital_output	select	NOR32_oc	T31	T29	T27	<b>AB</b>
out_lg	NC	out_probe	NC	Raz_Ch_n_p	Raz_Ch_n_n	Val_Evt_p	Val_Evt_n	PS_global_trig	NOR32T_oc	T30	T28	<b>AC</b>
<b>12</b>	<b>13</b>	<b>14</b>	<b>15</b>	<b>16</b>	<b>17</b>	<b>18</b>	<b>19</b>	<b>20</b>	<b>21</b>	<b>22</b>	<b>23</b>	

Figure 6 - South east Citiroc1A ball-out



# Datasheet Citiroc1A



## DIMENSIONS

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A			1.20
A1	0.15		
A2		0.88	
A3		0.28	
b	0.25	0.30	0.35
D	11.85	12.00	12.15
D1		11.00	
e		0.50	
E	11.85	12.00	12.15
E1		11.00	
F		0.50	
ddd			0.08
eee			0.15
fff			0.05

Figure 7 - Citiroc1A TFPGA353 mechanics



## 3 ASIC programmable parameters

### 3.1 General description

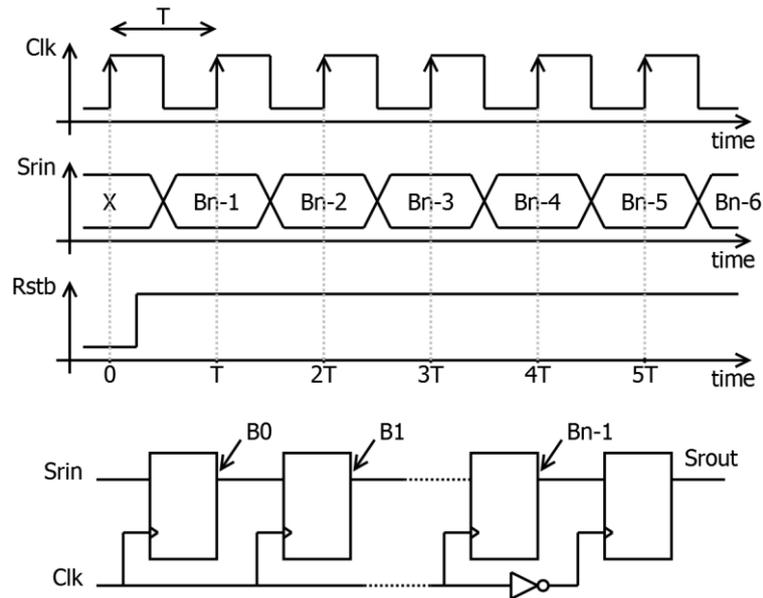


Figure 8: Slow control chronogram and explanation.

The slow control is a shift register composed of 1144 flip flops (first bit is  $B_0 = DAC\_t<0>$  and last is  $B_{1143} = EN\_32$  triggers). Data are stored in flip-flops on leading edge of the clock. The data are shifted at each clock cycle as seen on Figure 8. Between  $srou$  and the output of the last slow control register's flip flop, there is another flip flop clocked on  $!clk$  so an additional falling edge is needed to send the data out on  $Srou$ .

### 3.2 Slow control register parameters

Register Name	bits	Register description	Subadd
Channel 0 to 31 4-bit_t	128	Ch0 to 31 4-bit DAC_t ([0..31])	0
Channel 0 to 31 4-bit	128	Ch0 to 31 4-bit DAC ([0..31])	128
EN_discri	1	Enable Discriminator	256
PP: Discriminator	1	Disable trigger discriminator power pulsing mode (force ON)	257
GC: RS_or_discri	1	Select latched (RS : 1) or direct output (trigger : 0)	258
EN_discri_t	1	Enable Discriminator Two	259
PP: Discriminator_t	1	Disable trigger discriminator power pulsing mode (force ON)	260
EN_4b_dac	1		261
PP: 4b_dac	1		262
EN_4b_dac_t	1		263
PP: 4b_dac_t	1		264
DM: Discriminator Mask	32	Allows to Mask Discriminator (channel 0 to 31) [active low]	265
PP: HG T&H (Widlar SCA)	1	Disable High Gain Track & Hold power pulsing mode (force ON)	297
EN_HG_T&H (Widlar SCA)	1	Enable High Gain Track & Hold	298
PP: LG T&H (Widlar SCA)	1	Disable Low Gain Track & Hold power pulsing mode (force ON)	299
EN_LG_T&H (Widlar SCA)	1	Enable Low Gain Track & Hold	300
GC: SCA bias	1	SCA bias (1 = weak bias, 0 = high bias 5MHz ReadOut Speed)	301
PP: HG Pdet	1		302
EN_HG_Pdet	1		303
PP: LG Pdet	1		304



# Datasheet

## Citiroc1A



EN_LG_Pdet	1		305
Sel SCA or PeakD HG	1		306
Sel SCA or PeakD LG	1		307
bypass PSC	1	Bypass Peak Sensing Cell	308
Sel Trig Ext PSC	1		309
PP: Fast Shapers Follower	1	Disable fast shaper follower power pulsing mode (force ON)	310
EN_Fast Shaper	1	Enable fast shaper	311
PP: Fast Shaper	1	Disable fast shaper power pulsing mode (force ON)	312
PP: Low Gain Slow Shaper	1	Disable low gain slow shaper power pulsing mode (force ON)	313
EN_Low_Gain_Slow Shaper	1	Enable Low Gain Slow Shaper	314
GC : Time Constant LG Shaper	3	Low gain shaper time constant commands (2...0) [active low]	315
PP: High Gain Slow Shaper	1	Disable high gain slow shaper power pulsing mode (force ON)	318
EN_High_Gain_Slow Shaper	1	Enable high gain Slow Shaper	319
GC : Time Constant HG Shaper	3	High gain shaper time constant commands (2...0) [active low]	320
GC : LG PA bias	1	Low Gain PreAmp bias ( 1 = weak bias, 0 = normal bias)	323
PP: Low Gain PreAmplifier	1	Disable Low Gain preamp power pulsing mode (force ON)	324
EN_Low_Gain_PA	1	Enable Low Gain preamp	325
PP: High Gain PreAmplifier	1	Disable High Gain preamp power pulsing mode (force ON)	326
EN_High_Gain_PA	1	Enable High Gain preamp	327
GC : Fast Shaper on LG	1	Select LG PA to send to Fast Shaper	328
EN_input_dac	1	Enable 32 input 8-bit DACs	329
GC : 8-bit DAC reference	1	8-bit input DAC Voltage Reference (1 = internal 4,5V , 0 = internal 2,5V)	330
ID Input 8-bit DAC	288	Input 8-bit DAC Data from channel 0 to 31 – (DAC7...DAC0 + DAC ON)	331
Channel 0 to 31 PA	480	Ch0 to 31 PreAmp config (HG gain[0..5], LG gain [0..5], CtestHG, CtestLG, PA disabled)	619
PP: Temp	1	Disable Temperature Sensor power pulsing mode (force ON)	1099
EN_Temp	1	Enable Temperature Sensor	1100
PP: BandGap	1	Disable BandGap power pulsing mode (force ON)	1101
EN_BandGap	1	Enable BandGap	1102
EN_DAC1	1	Enable DAC1	1103
PP: DAC1	1	Disable DAC1 power pulsing mode (force ON)	1104
EN_DAC2	1	Enable DAC2	1105
PP: DAC2	1	Disable DAC2 power pulsing mode (force ON)	1106
GC : DAC1 code	10	10-bit DAC1 (MSB-LSB)	1107
GC : DAC2 code	10	10-bit DAC2 (MSB-LSB)	1117
EN_High Gain OTAq	1	Enable High Gain OTA	1127
PP: High Gain OTAq	1	Disable High Gain OTA power pulsing mode (force ON)	1128
EN_Low Gain OTAq	1	Enable Low Gain OTA	1129
PP: Low Gain OTAq	1	Disable Low Gain OTA power pulsing mode (force ON)	1130
EN_Probe OTAq	1	Enable Probe OTA	1131
PP: Probe OTAq	1	Disable Probe OTA power pulsing mode (force ON)	1132
Testb_Otaq	1	Otaq test bit	1133
EN_Val_Evt receiver	1	Enable Val_Evt receiver	1134
PP: Val_Evt receiver	1	Disable Val_Evt receiver power pulsing mode (force ON)	1135
EN_Raz_ChN receiver	1	Enable Raz_ChN receiver	1136
PP: Raz Chn receiver	1	Disable Raz Chn receiver power pulsing mode (force ON)	1137
EN_out_dig	1	Enable digital multiplexed output (hit mux out)	1138
EN_OR32	1	Enable digital OR32 output	1139
EN_NOR32_oc	1	Enable digital OR32 Open Collector output	1140
Trigger Polarity	1		1141
EN_NOR32T_oc	1	Enable digital OR32_T Open Collector output	1142
EN_32 triggers	1	Enable 32 channels triggers outputs	1143



Total	1144	1144
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Table 4 – slow control register parameters

### 3.3 Probe register parameters

An analogue probe output is available for the debug of the Citiroc 1. This output is set by the probe register; refer to the truth table below. This "probe" register shares the same I/O with the "slow control" register as both are multiplexed. Selection of either "probe" or "slow control" is done by the "Select" pin.

For each of the 32 channels, output of low and high gain preamplifier, of low gain and high gain slow shaper, of fast shaper and the internal signals "PeakSensing\_modeb\_LG" and "PeakSensing\_modeb\_HG" can be monitored.

Only one analogue and one digital output can be chosen at the same time.

In normal use, this probe output should be disabled by Slow Control to save power.

Signal name	Probe	Comments	Subadd	
Out_fs	32	From channel 0 to 31	0	Analog
Out_ssh_LG	32	From channel 0 to 31	32	Analog
PeakSensing_modeb_LG	32	From channel 0 to 31	64	Digital
Out_ssh_HG	32	From channel 0 to 31	96	Analog
PeakSensing_modeb_HG	32	From channel 0 to 31	128	Digital
Out_PA_HG/Out_PA_LG	64	From channel 0 to 31	160	Analog
<b>Total</b>	<b>224</b>		<b>224</b>	

Table 5 – Probe register parameters

## 4 ASIC Front-end

### 4.1 Input DACs

The chip is foreseen to be connected to an external power supply and to provide a common forward high voltage to all connected 32 SiPM. Tuning of the applied voltage, channel by channel, is achieved using a high impedance output 8-bit DAC dedicated to each detector power line. A slow control bit permits to use either the 2.5V internal reference or a 4.5V external reference as dynamic range for this High Voltage tuning. The input DACs have 9 control bits: 1 to enable/disable the DAC and 8 to set voltage. Whenever 2.5V dynamic range is used, an external resistor to GND is needed to adjust the slope of these DACs on pin "iref\_dac\_5V".

Note: to perform a linearity test of these input DACs, a very high impedance multimeter is required (~1Gohm).



# Datasheet Citiroc1A

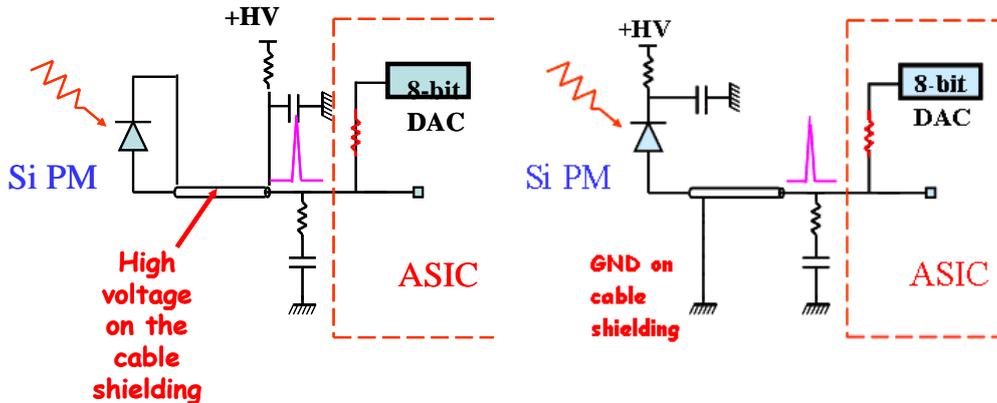


Figure 9 – 2 different schemes of the SiPM connection to the ASIC

## 4.2 Preamplifiers

Each channel of CITIROC embeds two channel-by-channel independent programmable variable-gain preamplifiers ensuring a versatile coverage of the dynamic range depending on the application. Both low gain and high gain preamplifier can be tuned on 6 bits ( $C_f$  can be tuned from 0 to 1575fF with a step of 25fF). The voltage gain is given by  $C_{in}/C_f$ ,  $C_{in}=15pF$  for high gain and 1.5pF for low gain

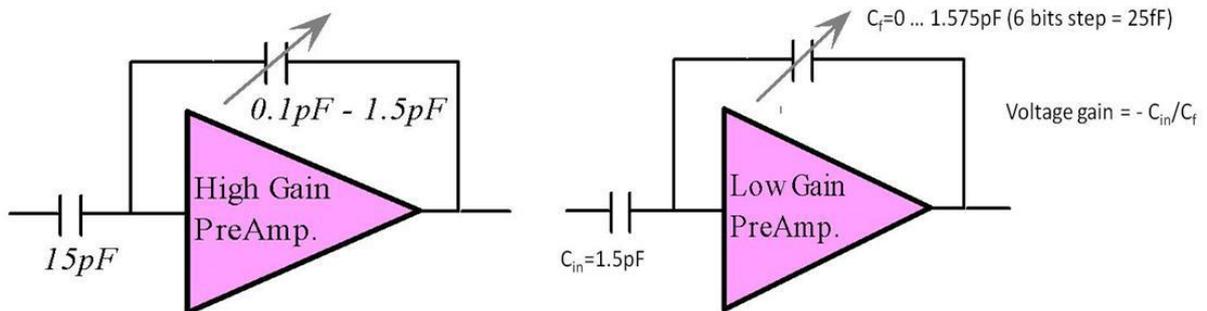


Figure 10 – High gain and low gain voltage sensitive preamplifier

Any channel preamplifier can be shut down by slow control bit ("disable PA"), to disconnect any noisy channel from the system.

A calibration input is included in each channel and can be enabled individually by slow control parameters ("In\_calib enabled"). In order to have a good precision, only one calibration input should be allowed at the same time. The injection calibration capacitance value is about 3pF.

Linearity of Low Gain preamplifier can be improved by increasing its current consumption. The slow control bit "Low Gain PreAmp Bias" controls that feature.

## 4.3 Slow Shaper

A CRRC· slow shaper is integrated to provide a charge measurement. The peaking time can be tuned thanks to the slow control parameters. Seven CRRC· shaping times (from 12.5 ns to 87.5 ns) are available for these slow shapers.

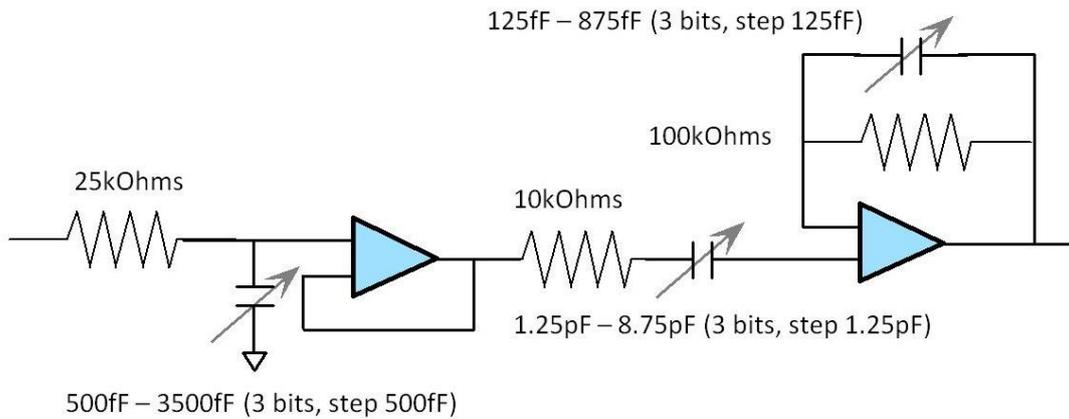


Figure 11 – Slow shaper schematic

Slow control value	Peaking time value
1 (001)	12.5 ns
2 (010)	25.0 ns
3 (011)	37.5 ns
4 (100)	50.0 ns
5 (101)	62.5 ns
6 (110)	75.0 ns
7 (111)	87.5 ns

Table 6– Slow shaper peaking time value vs slow control parameters

#### 4.4 Trigger line

A dedicated 15ns peaking-time fast shaper can either be connected to the high gain preamplifier or to the low gain. That connection is set by slow control.

This shaper signal is then compared to a threshold, thanks to a discriminator which provides the trigger signal. There are two discriminators in Citiroc1A:

- The first one provides the trigger (OR32) and is also used for the “hit register”. The discriminators outputs provide trigger signals which give the OR32. These outputs can be latched by slow control command (“RS\_or\_discr”). The reset of the latched (if used) triggers is performed by the LVDS signal “Raz\_Ch”.n”.
- The second one provides the event time information on each channel. Indeed, the 32 discriminators outputs are available.



# Datasheet Citiroc1A

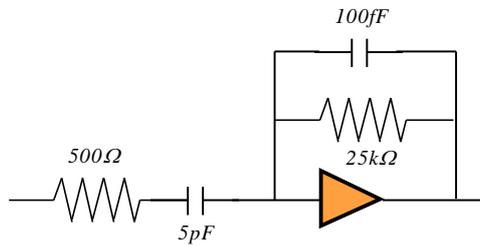


Figure 12 – Fast Shaper schematic

Thresholds are set by two internal 10-bit DAC common to the 32 channels allowing threshold to be tuned coarsely from 1.1V up to 2.4V with a step of 1.3mV, and then be set channel by channel by an individual 4-bit DAC allowing threshold to be tuned finely around the coarse value. The slow control register sets these thresholds.

Any channel trigger can be quiet by slow control using the “Mask discriminator” setting. It mutes a precise channel output and its contribution to the OR32 signal.

To activate the digital part of this ASIC, an acquisition window has to be enable. This is done by the LVDS signal “Val\_Evt”.

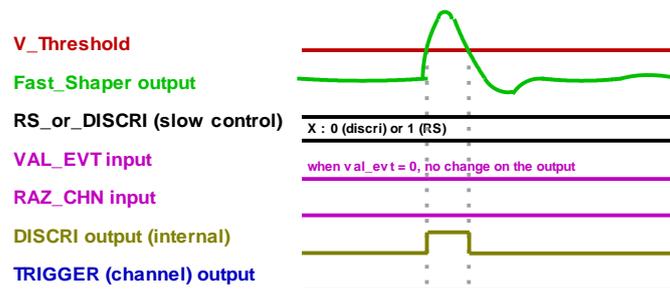


Figure 13 – Val Evt signal effect

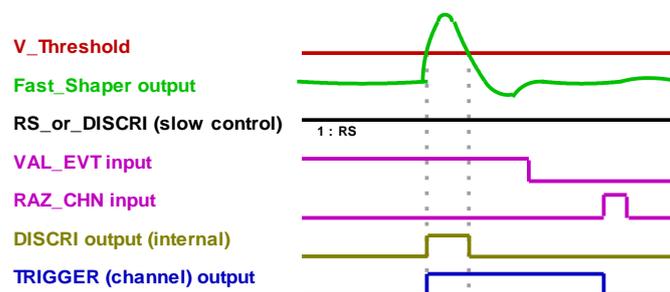


Figure 14 – Trigger output using Latch



# Datasheet Citiroc1A

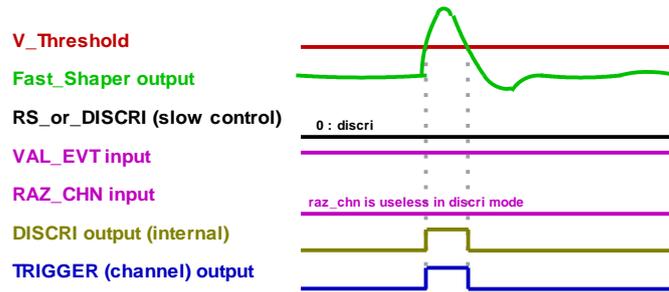


Figure 15 – Trigger output in direct discriminator mode

## 4.5 Track and hold

The chip has to save the amplitude of the pre-amplified and shaped signal at its peaking time. This is achieved using a track and hold cell. This hold control signal is directly provided to the ASIC by the user on a dedicated pin (*holdb\_hg* for high gain and *holdb\_lg* for low gain). This hold command is active low. Analogue data is stored at the same time on low gain SCA and high gain SCA.

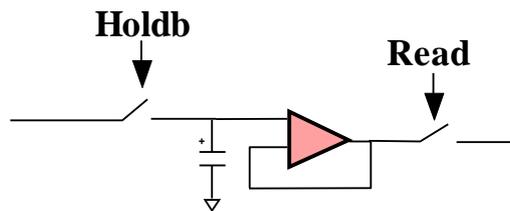


Figure 16 – Schematic of track and hold cell

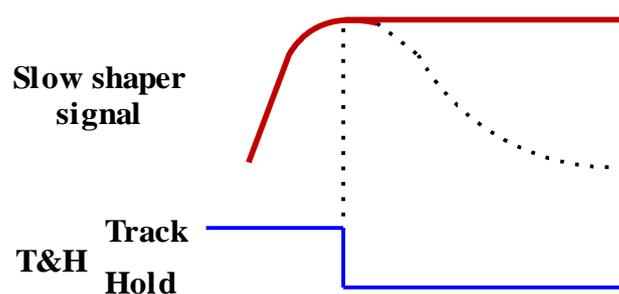


Figure 17– Standard Track & Hold working mode

The readout of these analogue memories is controlled by the read register. The readout speed is limited to 2 MHz by these Track & Hold cells (SCA cells). However, in order to save maximum power, a slow control bit ("T&H bias") permits to decrease current flowing in these cells, resulting a maximum readout speed to 600 kHz.



# Datasheet Citiroc1A



## 4.6 Peak detector

In parallel of standard track and hold, a peak detector has been implemented to store the analogue data. The peak detector is controlled by 3 digital signals. These signals are "THb", "Trig" and "Rstb".

- "Rstb" is the reset signal;
- "Trig" is the discriminator output provided internally or externally;
- "THb" is the discriminator output delayed provided externally on the pins "holdb\_hg" for high gain path and "hold\_lg" for low gain path. The delay equals the shaping time on the charge measurement channel.

When nothing happens, the peak detector is in track mode: it works like a voltage follower. When a signal is detected on the trigger channel, the peak detector receives the "Trig" signal and it switch to peak detector mode. To avoid any glitch or pile-up during the readout, the output is open thanks to the THb signal. The THb signal must fire after the peak of the shaper and before the beginning of the readout without ant particular precision in timing.

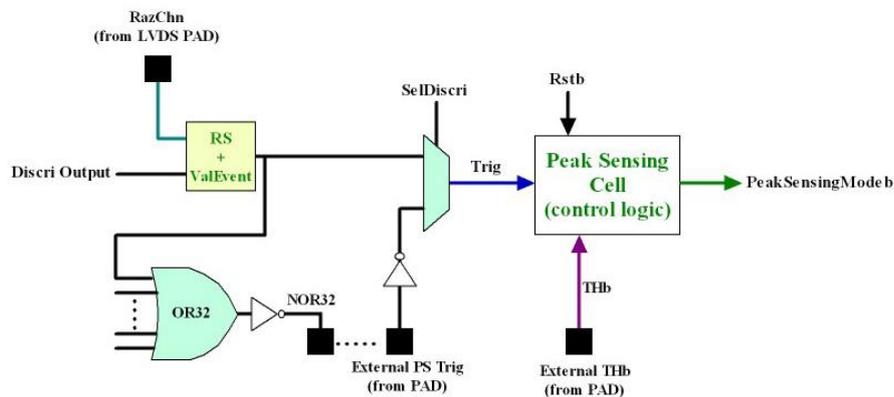
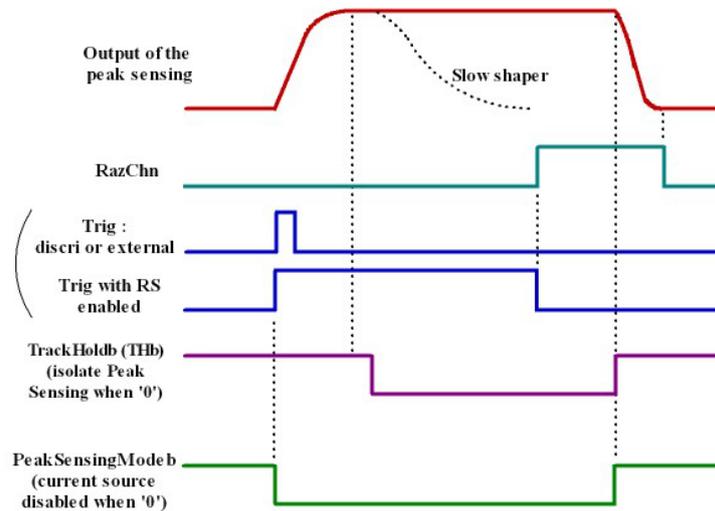


Figure 18 – Peak detector working mode



## 5 ASIC Back-end

### 5.1 Direct digital Outputs

4 different outputs are available in parallel on this chip:

- OR32: a cabled OR of all channels triggers
- OR32\_t: a cabled OR of all channels triggers
- 32 Triggers: each channel trigger on a pin

The buffers of these digital outputs are powered between VHI (for logic "1") and VLO (for logic "0"). Thus, these pins need a supply voltage when the outputs are required.

Note that VLO must be greater or equal to GND (0V) and VHI smaller or equal to VDD (3.3V).

### 5.2 Analogue chip read out

The 2 analogue outputs (low gain & high gain outputs) can be read by selecting the channel using the Read register. (See below on the "Multiplexed outputs description" section). Note that when no channel is selected, the outputs are set in high impedance, allowing multiple ASICs to share a common line for each gain output.

When no channel is selected, an OR function of the contents of this "read" register ensures high impedance the 3 outputs (low gain, high gain and digital output).

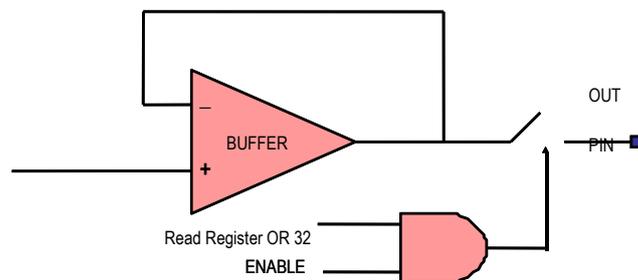


Figure 19- Read Register

This architecture of the "read" register and on the analogue (and hit) outputs allows sharing same line for the data which is read sequentially for multiples ASICs.

### 5.3 Output (Multiplexed Latches): Hit Register

One high impedance digital output can provide the trigger of each channel sequentially. This requires the use of Latch in the discriminator cell. The readout of this register is complete in parallel with the readout of the charge measurement (low gain and high gain).

The buffer of this digital output is powered between VHI (for logic "1") and VLO (for logic "0").



## Multiplexed LG Charge, HG Charge & Hit outputs

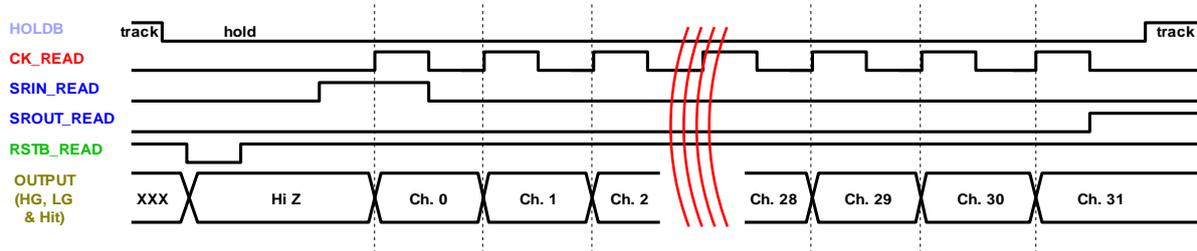


Figure 20 – Read Register

### 5.4 Power pulsing and ON/OFF functions

Each unused stage can be disabled to reduce power consumption. This is controlled by the slow control bits “Enable”. Moreover, in order to save more power, chosen chip stages can be switched off dynamically thanks to the “pwr\_on” command (provided by a pin). This mode is the power pulsing function. Caution, for each stage, the slow control bit “Power Pulsing” allows to bypass this feature by forcing it ON. (Refer to the truth table below).

Note that turning OFF a stage has the highest priority.

Slow Control : EN	Slow Control : PP	Input PIN : pwr_on	Comments
0	X	X	Stage disabled
1	0	OFF / 0	Power pulsing mode : Stage shut down
1	0	ON / 1	Power pulsing mode : Stage powered
1	1	X	Stage powered

Table 7 – Power mode truth table